

I claim:

- 1 1. An apparatus, comprising:
2 execution logic to execute a load instruction with a predicted load value; and
3 a table coupled to the execution logic and having a first field to store the
4 predicted load value, the table to be used in repairing a mis-prediction of
5 the predicted load value after a cache miss caused by a request of an
6 actual load value.

- 1 2. The apparatus of claim 1, wherein:
2 the execution logic is to execute the load instruction with the actual load value
3 responsive to a cache hit caused by execution of the load instruction.

- 1 3. The apparatus of claim 1, wherein:
2 the table includes a miss status holding register.

- 1 4. The apparatus of claim 1, wherein:
2 the table includes a second field to indicate a destination register for the load
3 instruction.

- 1 5. The apparatus of claim 1, wherein:
2 the table includes a second field to store an address identifying a location of the
3 actual load value.

1 6. A system, comprising:
2 a main memory;
3 a cache memory coupled to the main memory;
4 instruction execution logic coupled to the cache memory to execute a load
5 instruction with an actual load value if a request of the actual load value
6 results in a cache hit and to execute the load instruction with a predicted
7 load value if the request of the actual load value results in a cache miss;
8 and
9 a table coupled to the instruction execution logic and having a first field to store
10 the predicted load value if the request of the actual load value results in
11 the cache miss.

1 7. The system of claim 6, wherein:
2 the table includes a miss status holding register.

1 8. The system of claim 6, wherein:
2 the instruction execution logic is further to execute a check instruction to
3 compare the predicted load value from the first field with the actual load
4 value.

1 9. The system of claim 8, wherein:
2 the instruction execution logic is further to branch to repair code if the predicted
3 load value is different than the actual load value.

1 10. The system of claim 6, wherein:
2 the table is to not store the predicted load value if the request for the actual load
3 value results in the cache hit.

1 11. An apparatus, comprising:
2 a processor to execute an instruction set including
3 a first set of one or more instructions to load a predicted load value and
4 to place the predicted load value in a table in response to an
5 attempt to load an actual load value resulting in a cache miss;
6 and
7 a second set of one or more instructions to compare the predicted load
8 value from the table with the actual load value and branch to
9 repair code if the actual load value is different than the predicted
10 load value.

1 12. The apparatus of claim 11, wherein:
2 the first set is to not place the predicted load value in the table in response to the
3 attempt to load the actual load value resulting in a cache hit.

1 13. The apparatus of claim 11, wherein:
2 the second set is to examine the table to determine if the table includes the
3 predicted load value.

1 14. The apparatus of claim 11, wherein:
2 the first and second sets are to be specified by a compiler.

1 15. The apparatus of claim 11, wherein:
2 the first and second sets are to be specified during execution.

1 16. A method, comprising:
2 executing a load instruction using a predicted load value responsive to a cache
3 miss resulting from an attempt to execute the load instruction with an
4 actual load value;
5 placing the predicted load value in a table;
6 retrieving the actual load value;
7 comparing the actual load value with the predicted load value in the table to
8 determine if the predicted load value was mis-predicted; and
9 re-executing at least one of the load instruction and load-dependent instructions
10 using the actual load value if the predicted load value was mis-predicted.

1 17. The method of claim 16, wherein:
2 said comparing includes comparing after the load instruction is retired.

1 18. The method of claim 16, wherein:
2 said placing includes placing the predicted load value in a miss status holding
3 register.

1 19. A machine-readable medium that provides instructions, which when executed
2 by a set of one or more processors, cause said set of processors to perform operations
3 comprising:

4 executing a load instruction using a predicted load value responsive to a cache
 5 miss resulting from an attempt to execute the load instruction with an
 6 actual load value;
 7 placing the predicted load value in a table if said attempt results in a cache miss;
 8 comparing the actual load value with the predicted load value from the table to
 9 determine if the predicted load value was mis-predicted; and
 10 re-executing at least one of the load instruction and load-dependent instructions
 11 using the actual load value if the predicted load value was mis-predicted.

1 20. The medium of claim 19, wherein:
 2 said re-executing includes branching to repair code.

1 21. The medium of claim 19, wherein:
 2 said comparing includes determining if the table includes an entry
 3 corresponding to the load instruction.

1 22. The medium of claim 19, wherein:
 2 said placing includes placing the predicted load value in a miss status holding
 3 register.

1 23. A method, comprising:
 2 generating first code to load an actual load value if requesting the actual load
 3 value results in a cache hit, and to load a predicted load value and place
 4 the predicted load value in a table if requesting the actual load value
 5 results in a cache miss;

6 generating second code to compare the predicted load value from the table with
 7 the actual load value; and
 8 generating third code to execute at least one of a load instruction and a load-
 9 dependent instruction with the actual load value.

1 24. The method of claim 23, wherein:
 2 said generating the second code includes generating code to determine if the
 3 table includes an entry generated by the first code.

1 25. The method of claim 23, wherein:
 2 said generating the third code includes generating code to be executed if
 3 executing the second code determines the predicted load value is
 4 different than the actual load value.

1 26. The method of claim 23, further comprising:
 2 generating said first, second, and third code only if it is determined that said
 3 requesting the actual load value is likely to result in a cache miss.

1 27. A machine-readable medium that provides instructions, which when executed
 2 by a set of one or more processors, cause said set of processors to perform operations
 3 comprising:
 4 generating first code to load an actual load value if requesting the actual load
 5 value results in a cache hit, and to load a predicted load value and place
 6 the predicted load value in a table if requesting the actual load value
 7 results in a cache miss;

8 generating second code to compare the predicted load value from the table with
 9 the actual load value; and
 10 generating third code to execute at least one of a load instruction and a load-
 11 dependent instruction with the actual load value.

1 28. The medium of claim 27, wherein:
 2 said generating the second code includes generating code to determine if the
 3 table includes an entry generated by the first code.

1 29. The medium of claim 27, wherein:
 2 said generating the third code includes generating code to be executed if
 3 executing the second code determines the predicted load value is
 4 different than the actual load value.

1 30. The medium of claim 27, further comprising:
 2 generating said first, second, and third code only if it is determined that said
 3 requesting the actual load value is likely to result in a cache miss.